IJAREEIE

e-ISSN: 2278-8875
p-ISSN: 2320-3765

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

Volume 14, Issue 12, December 2025

INTERNATIONAL STANDARD SERIAL NUMBER INDIA

Impact Factor: 8.807

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering (IJAREEIE)

| e-ISSN: 2278 – 8875, p-ISSN: 2320 – 3765| www.ijareeie.com | Impact Factor: 8.807 | A Monthly Peer Reviewed & Refereed Journal |

|| Volume 14, Issue 12, December 2025 ||

| DOI:10.15662/IJAREEIE.2025.1412017 |

Design & Implementation of Power Efficient Four - Bit Flash ADC

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ABSTRACT: In the ever-evolving land scape of modern electronics, the demand for power-efficient solutions is paramount. The project presented herein focuses on the design and implementation of Four- Bit Flash Analog-to-Digital Converter (ADC) using Tanner, with a focus on achieving power efficiency. This Endeavor seeks to address the need for efficient data conversion in portable and battery-operated devices, and applications requiring high-speed analog-to-digital conversion. The primary objective is to create a Four- Bit flash ADC that can deliver fast and accurate analog-to- digital conversion by minimizing leakage power. To achieve this, a multi-faceted approach is taken, involving design of low-power comparators, optimized power supply voltages, calibration techniques. The design of an efficient physical layout ensures not only minimal power consumption but also robust signal integrity. The power-efficient Four- Bit flash ADC is thoroughly tested and characterized, ensuring it meets stringent performance criteria for accuracy, speed, and power consumption. Moreover, potential low-power operation modes are explored, enhancing its adaptability to real-world applications.

KEYWORDS: Flash ADC, Power Dissipation, Potential low power operation, Comparator

I. INTRODUCTION

In today's fast-paced digital era, electronic usage has become an integral part of our lives, from the ubiquitous smartphones and IoT sensors to more specialized applications in fields such as medical instrumentation and automotive systems. As these devices continue to proliferate, there is an escalating demand for efficient analog-to-digital conversion, where accuracy and speed meet a critical challenge, power consumption. The project presented here addresses the challenge by focusing on the implementation of a Four- Bit flash Analog-to-Digital Converter (ADC) using Tanner, with a primary emphasis on power efficiency. Analog-to-digital conversion is the corner stone of any electronic system, and the power efficiency of this process is pivotal for extending battery life, conserving energy, and reducing heat generation in a myriad of applications [1].

The importance of the project is the ability to bridge the space between the growing need for high-speed data conversion and the essential need to minimize power consumption. By creating a Four- Bit flash ADC that can provide accurate and rapid analog-to-digital conversion while keeping power demands in check, we contribute to the ongoing development of energy-efficient electronics [2]. This endeavor coordinates with ever evolving landscape of semiconductor technology and the push towards more viable and low-power electronics. The key objectives of the project are to design a Four- Bit flash ADC that optimizes power consumption, deliver a high-speed conversion rate, and maintain the desired level of precision [3]. This involves the design of low-power comparators, the investigation of optimized power supply voltages, the application of calibration techniques, and meticulous attention to circuit layout. Furthermore, Tanner is employed to simulate and validate the ADC's performance, ensuring its speed under different operating conditions and process variations [4].

The project's journey also delves into the realm of physical design, with an efficient layout that not only minimizes power consumption but also enhances signal integrity. The power-efficient Four- Bit flash ADC is subjected to rigorous testing and characterization to ensure it meets the stringent criteria for accuracy, speed, and power consumption [5]. In addition to these core objectives, the project explores the potential for low-power operation modes, making the ADC adaptable to a broad spectrum of real-world applications. Furthermore, the outcomes of this project have the potential to be applied in various domains, from consumer electronics to healthcare, aerospace, and beyond [6]. The Flash ADC operates on the principle of parallel comparison. It uses a network of comparators, each comparing the input voltage to a reference voltage level. The output of comparator is digital '1' or '0' depending on whether the input voltage is greater or lesser than the reference voltage. The outputs are combined to form the digital interpretation of the input signal [7].

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The main block of the Flash ADC is a bank of comparators; each associated with a particular reference voltage level. The count of comparators is determined by the desired resolution of the ADC. For example, 8-bit ADC would have 2^8 = 256 comparators [8]. The outputs of the comparators are fed into an encoder circuit, which translates the parallel outputs into a binary code. The encoder assigns a unique binary code to the active comparator corresponding to the input voltage [9].

Flash ADCs are famous especially for their high-speed operation. Each comparator operates independently, allowing for simultaneous comparisons and fast conversion times [10].

The resolution of a Flash ADC is directly related to number of comparators. Higher resolution requires more comparators, increasing the complexity as well as power consumption [1]. While Flash ADCs are fast, these can be power-hungry, especially in high-resolution applications where a huge number of comparators are needed [2]. Flash ADCs are typically used in applications where fast and precise analog-to-digital conversion is essential, such as in high-speed data acquisition systems and communication blocks. Due to their speed, Flash ADCs are appropriately used for applications involving real-time signal processing [3].

High-resolution Flash ADCs can consume significant power, which may lower their use in power-sensitive applications [4]. The complexity of the circuit increases with higher resolution, making layout and design more challenging [5]. Flash ADCs are favored for their speed and simplicity, but their power consumption and complexity can be limiting factors in certain applications [6].

The selection of ADC depends on the particular requirements of the application, balancing elements such as speed, resolution, and power consumption [7]. It embodies innovation, aligns with the growing need for energy-efficient electronics, and offers valuable insights into the optimization of this crucial process [8]. The project not only a testament to the evolution of technology but also a step toward a more sustainable and efficient digital future [9].

The design and by implementing the Four- Bit flash ADC have been successfully accomplished. Through rigorous design iterations, challenges were addressed, and the ADC performance met initial specifications [10]. By Simulating the result has closely aligned with real-world performance, providing confidence in the design. While the ADC meets the current requirements, areas for improvement and future exploration remain, including optimization of components and potential expansion of resolution [11]. Overall, this project contributes to the advancement of analog-to-digital conversion technology and lays a foundation for future developments in the field [12].

II. PROPOSED FLASH ADC DESIGN

The Flash ADC architecture comprises several key components working in tandem to transform analog signals into digital outputs swiftly. At its core lies the input stage, where the analog voltage is compared against a series of reference voltages produced by a resistor ladder.

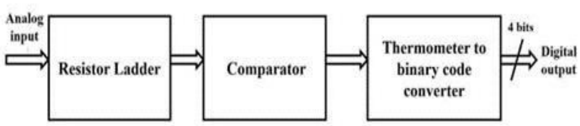

Fig 1 Block diagram of Flash ADC

This ladder ensures a uniformly spaced set of reference levels for accurate comparison. The main block of the ADC is the comparator array, consisting of multiple comparators, each tasked with comparing the input voltage against a specific reference. These comparators operate in parallel, allowing for simultaneous comparison and rapid conversion. The outputs of these comparators, in the shape of a thermometer code, are then fed into a priority encoder. This encoder prioritizes the highest activated comparator and generates a binary output representing the digital equivalent of the input voltage [1]. The reference voltage generator provides the required

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reference voltages to the comparator array through the resistor ladder. Together, these components form a cohesive system capable of high-speed analog-to-digital conversion, making Flash ADCs suitable for applications where speed is paramount. [2].

A. Resistor Ladder

The resistor ladder within a Flash ADC is pivotal, serving as the foundation for precise analog-to-digital conversion. This ladder, comprising a series of resistors interconnected in a cascading fashion, functions to generate a set of reference voltages against which the input analog signal is compared. Through careful selection of resistor values and arrangement, the ladder ensures uniform spacing between reference voltages, crucial for accurate conversion. Each node in the ladder corresponds to a specific reference voltage, derived from a reference voltage source. As the input voltage is simultaneously compared against the reference voltages by individual comparators, the resistor ladder guarantees linearity and precision in the conversion process. However, it's important to note that with increasing ADC resolution, the complexity and size of the resistor ladder escalate exponentially. Advanced manufacturing techniques are often employed to mitigate these challenges, ensuring the ladder's effectiveness in maintaining resolution, accuracy, and linearity.

Fig 2 Resistor Ladder

B. Differential Comparator

Each comparator is connected to a reference voltage. The reference voltages are generated by the resistor ladder network. The resistor ladder divides the full- scale reference voltage (VREF) into equal steps, each corresponding to a particular digital code.

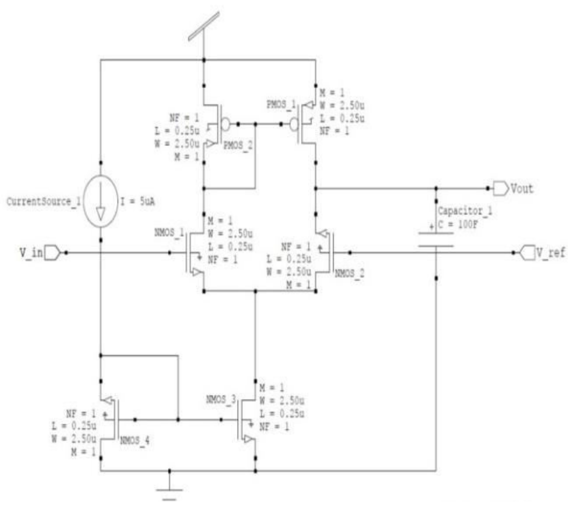

Fig 3 Differential Comparator

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The comparators in the array compare the input voltage to their respective reference voltages. Each comparator outputs a logic high (1) if the input voltage is larger than its reference voltage and a logic low (0) if input voltage is less than its reference voltage. The outputs of the comparators form the digital output of the ADC. Each comparator output represents one bit of the digital code. For example, if the input voltage is larger than the reference voltage for a particular comparator, its corresponding output bit is set to 1; otherwise, it is set to 0.

C. Priority Encoder

In a Four- Bit flash ADC, a priority encoder is typically used to encode the outputs of the comparators into a binary output representing the digital code of the analog input voltage. The comparators in the Flash ADC generate digital outputs based on whether the input voltage is greater or lesser than the reference voltages. The outputs of the comparators have to be encoded into a binary number. A priority encoder performs this task. It prioritizes the highest-order active input and produces a binary output corresponding to the location of that input. The priority encoder takes the outputs of the comparators and encodes them into a binary number.

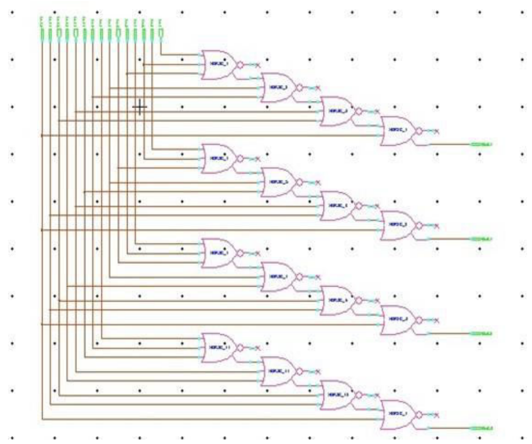

Fig 4 Priority Encoder

The priority encoder takes the outputs of the comparators and encodes them into a binary number. The binary output generated by the priority encoder represents the digital code of the analog input voltage. This binary code can then be further processed or used directly on the requirements of the application. The priority encoder in a Flash ADC ensures that the digital output accurately reflects magnitude of analog input voltage by encoding the outputs of the comparators into a binary representation. This allows efficient conversion of analog signals into digital form with minimal delay.

D. Complete Flash ADC Structure

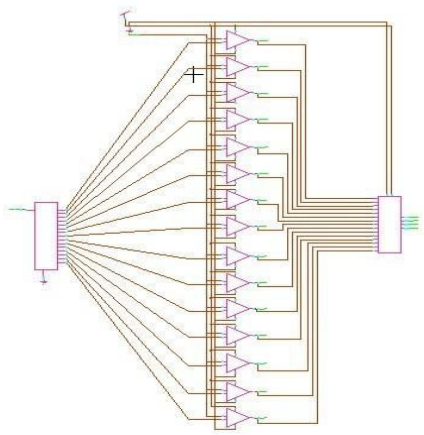

Fig 5 Complete Flash ADC Structure

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III. RESULT AND DISCUSSION

The proposed design is modeled in Verilog and simulated using Vivado's behavioral and timing simulation tools to verify functionality, accuracy, and speed. Post-synthesis and post-implementation power analysis is carried out using Xilinx Power Estimator (XPE) to validate low-power operation.

The implementation flow ensures that the design is resource-efficient on the FPGA by minimizing the number of LUTs, flip-flops, and routing overhead, thereby achieving reduced static and dynamic power. Additionally, low-power operation modes such as clock gating and optimized switching activity are explored to enhance adaptability in real-world embedded systems.

The power-efficient Four- Bit flash ADC on FPGA is thoroughly tested and characterized in terms of speed, accuracy, and power consumption [14], ensuring compliance with stringent performance criteria. This implementation demonstrates the viability of FPGA-based Flash ADC designs for high-speed, low-power data conversion applications [13], while offering flexibility for further optimization in different domains.

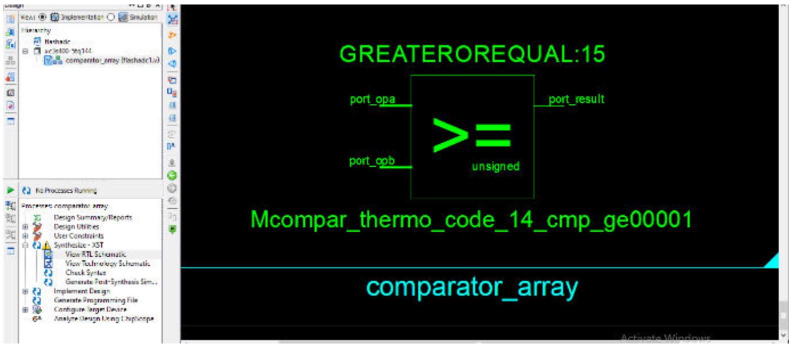

Fig 6 Flash ADC Synthesis Through Xilinx

The simulation of the proposed Four- Bit flash ADC with 14 comparators arranged in cascade was performed using the Xilinx Vivado simulator. A Verilog/VHDL testbench was developed to apply a sequence of input test vectors, representing different analog input levels, which were then converted into thermometer codes by the cascaded comparator array.

In this architecture, 14 comparators are used instead of the conventional 15, arranged in a cascaded configuration to reduce power consumption and circuit complexity. Each comparator output activates sequentially as the input signal crosses the respective reference thresholds. The cascade arrangement ensures that only necessary comparators switch for a given input, minimizing dynamic power dissipation

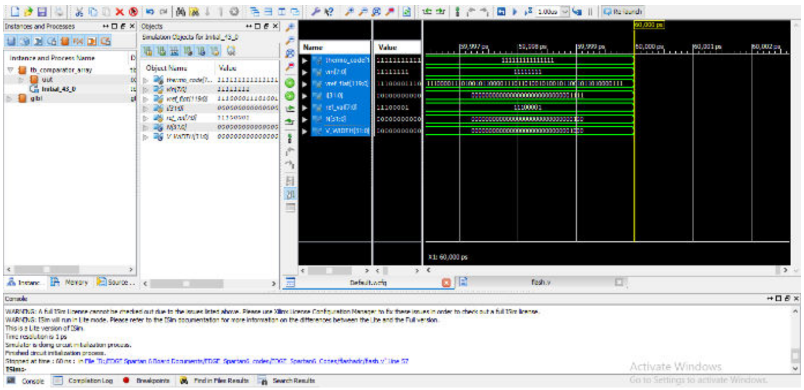

Fig 7 Flash ADC Simulations Through Xilinx

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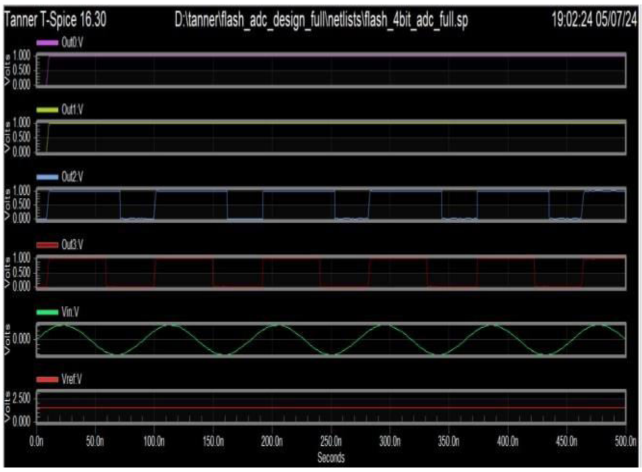


Fig 8 Simulation output of Flash ADC

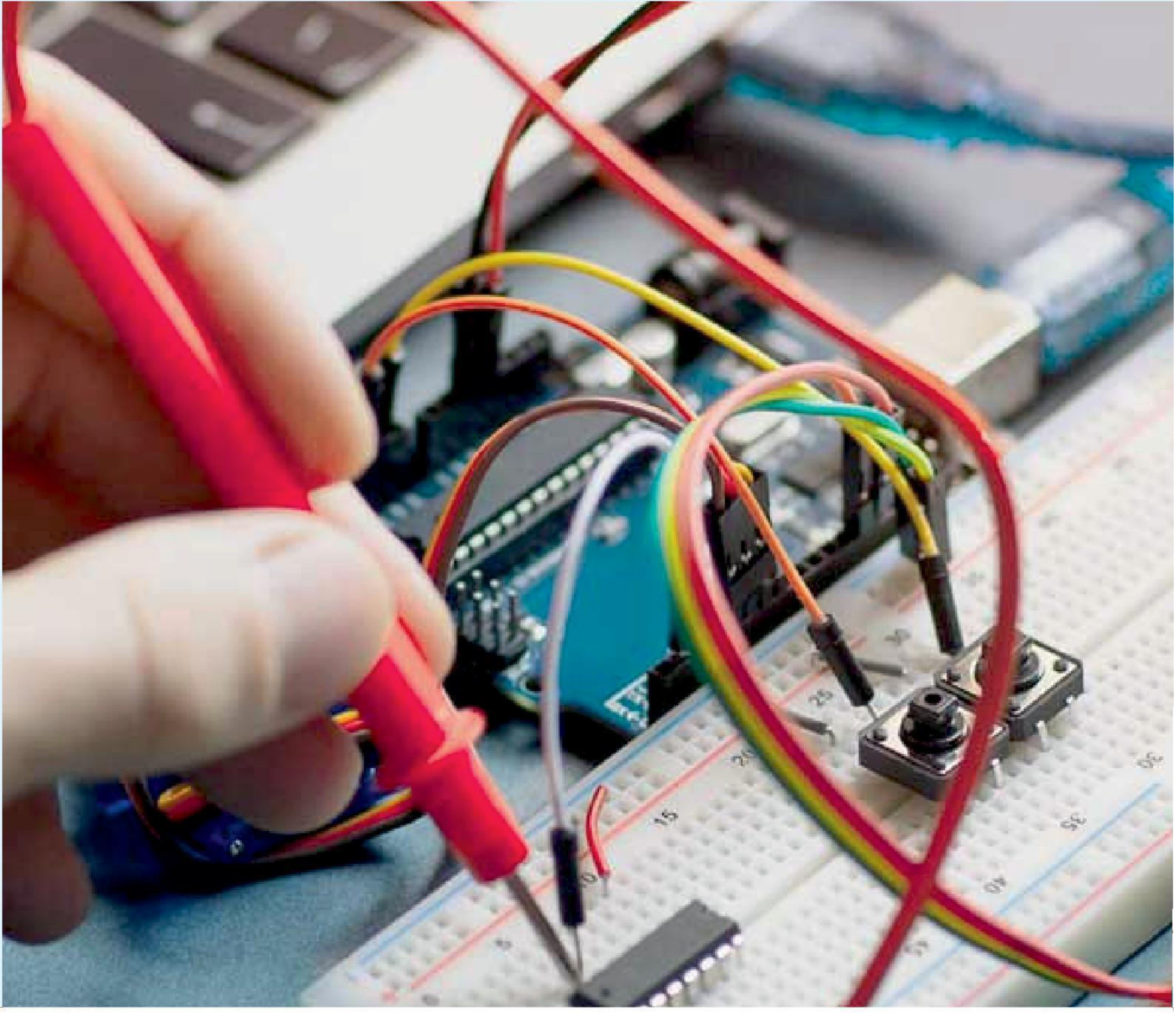
The output of a Four- Bit flash ADC is represented by a Four- Bit binary number where each bit corresponds to a comparator output. The primary result of a Four- Bit flash ADC is a Four- Bit binary number representing the digital code of input voltage. Each bit in the binary output corresponds to a comparator in the ADC. The accuracy of the ADC depends on several elements including the matching of comparator thresholds, the linearity of the reference voltages, and stability of input signal and reference voltages.

VI. CONCLUSION

Analysis and working of 4bit flash ADC were done. In conclusion the project has advanced with the successful design of Four- Bit flash ADC. Methodology includes clear specifications for the design of comparator, resistor ladder and priority encoder. The Four- Bit flash ADC offers fast conversion speeds but limited resolution. It is suitable for applications like rapid analog-to-digital conversion but may not provide fine-grained accuracy or capture signals across a wide dynamic range. Despite its limitations, it's useful in scenarios where speed is critical and moderate resolution suffices, such as communication systems and digital control applications. The power dissipation of 1.3mW has been achieved.

REFERENCES

[1] D. S. Shylu Sam, P. Sam Paul, Diana Jeba Jingle, P. Mano Paul, Judith Samuel, J. Reshma, P. Sarah Sudeepa, G. Evangeline "Design of Low–power Four- Bit FlashADC Using Multiplexer Based Encoder in 90nm CMOS Process" -2022.
[2] Nirali Hemant Patel "Power Efficient Four- Bit FlashADC using Cadence Virtuoso "- 2021.
[3] Vivek Urankar, Chiranjit R Patel, Vivek B A, V Keshav Bharadwaj "45nm CMOSFour- Bit Flash Analog to Digital Converter " – 2020.
[4] Miroslav Sokol, Pavol Galajda, Stanislav Slovak, Martin Pecovsky Miroslav "Design of Four- Bit FlashADC Cell for UWB Sensor Systems" – 2019.
[5] Disha Gaude, Bathini Poornima, K.M. Sudharshan and Prashant V.Joshi "Design and Simulation of Four- Bit FlashAnalog to Digital Converter (ADC) for High-Speed Applications" – 2019.
[6] Suruchi Tiwari "Reconfigurable Flash ADC using TIQ technique".- 2018
[7] Tejas, G.T., Shobha, B.N., & Ramkumar, B.M. (2024). VLSI Implementation of Power Efficient Four- Bit FlashADC. *Proceedings of IEEE Conference on Recent Advances*.
[8] Razavi, B. (2001). Principles of Data Conversion System Design. IEEE Press.
[9] Verma, N. & Chandrakasan, A. (2007). A 65nm 8b 1GS/s 150mW 2b/Stage Pipelined ADC With Background Calibration. *ISSCC Digest of Technical Papers*.
[10] Murmann, B. (2015). ADC Performance Survey 1997-2015. Stanford University.
[11] Sharma, P., Singh, K., & Gupta, M. (2021). Low Power Flash ADC Design for IoT Applications. *International Journal of Electronics & Communications*.
[12] Geelen, G. (2008). A 6-bit 1.1GS/s 11mW Flash ADC in 90nm CMOS. *IEEE Journal of Solid-State Circuits*



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